implant steps, leading to the advantage of lower cost than other techniques known in the art.

It is understood that additional fabrication processes may be performed to complete the fabrication of the semiconductor device shown in FIGS. **2-9**. For example, an interconnect structure containing a plurality of metal layers may be formed to establish electrical connections between components of the semiconductor device and external devices. Other processes such as passivation, wafer testing, wafer dicing, and packaging processes may also be performed.

One of the broader forms of the present disclosure involves a method. The method includes providing a substrate including a top surface. The method also includes forming a gate over the top surface of the substrate. The formed gate has a first height measured from the top surface of the substrate. The method also includes etching the gate to reduce the gate to a second height. This second height is substantially less than the first height.

Another one of the broader forms of the present disclosure also involves a method. The method includes providing a wafer including a top surface. The method also includes forming a first gate and a second gate over the top surface of the wafer. The method also includes performing an etching process on the first gate to reduce a height of the first gate while protecting the second gate. After this etching process, the height of the first gate is substantially less than a height of the second gate.

Another one of the broader forms of the present disclosure involves a semiconductor device. The semiconductor device includes a substrate. The substrate includes a top surface. The semiconductor device also includes a first gate formed over the top surface of the substrate. The first gate has a first height. The semiconductor device also includes a second gate formed over the top surface of the substrate. The second gate has a second height. The first height is substantially less than the second height.

The foregoing has outlined features of several embodiments so that those skilled in the art may better understand the detailed description that follows. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A method, comprising:

providing a substrate including a top surface;

forming a gate and gate spacers over the top surface of the substrate, the gate and gate spacers having a first height measured from the top surface of the substrate;

forming a patterned photoresist layer over the substrate, the photoresist layer covering portions of the substrate and exposing the gate, wherein the gate spacers have external side surfaces that are exposed at a point lower than a top of the gate; and

etching a gate electrode and the gate spacers of the gate with the photoresist layer present to reduce the gate to a second height, the second height being about 10% to about 75% of the first height.

2. The method of claim **1**, wherein the forming the gate includes forming an additional gate having a third height; and wherein after the etching the second height is substantially less than the third height.

3. The method of claim **2**, further including:

forming a resist protective oxide (RPO) layer over the gate; and

forming a silicide layer over the additional gate.

4. The method of claim **2**, wherein the gate includes a polysilicon material; and wherein the additional gate includes a material selected from polysilicon and metal.

5. The method of claim **2**, further including: forming different numbers of contacts on the etched gate and the additional gate.

6. The method of claim **2**, wherein the etching is carried out in a manner so that the additional gate is protected during the etching.

7. The method of claim **2**, wherein the substrate includes a shallow trench isolation (STI) device and an active region; and

wherein the gate is formed above the shallow trench isolation device and the additional gate is formed above the active region.

8. The method of claim **1**, further including:

performing an implant process on the gate;

wherein the implant process uses BF_2 as a dopant and has an implantation energy level between 10 KeV and 40 KeV and a dosage between 9×10^{14} ions/cm^2 and 4×10^{15} ions/cm^2.

9. A method, comprising:

providing a substrate including a top surface;

forming a first gate and gate spacers and a second gate and gate spacers over the top surface of the wafer;

forming a patterned photoresist layer over the substrate, the photoresist layer protecting the second gate and exposing the first gate, wherein external side surfaces of the gate spacers of the first gate are exposed and the gate spacers are a same height as the first gate; and

performing an etching process on a gate electrode and the gate spacers of the first gate to reduce a height of the first gate while protecting the second gate.

10. The method of claim **9**, wherein the etching reduces the height of the first gate to about 10% - 75% of the height of the second gate.

11. The method of claim **9**, further including:

performing an implant process on the first gate; wherein the implant process uses BF_2 as a dopant and has an implantation energy level between 10 KeV and 40 KeV and a dosage between 9×10^{14} ions/cm^2 and 4×10^{15} ions/cm^2.

12. The method of claim **9**, further including: forming a resist protective oxide layer on the first gate; and forming a silicide layer on the second gate.

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